Remarks

In the fifth, non-final Office Action, dated September 5, 2007, claim 21 was rejected under 35 U.S.C. 103(a) over U.S. Patent No. 5,926,710 to Tseng in view of U.S. Patent No. 6,010,931 to Sun et al. (hereafter, "Sun"). In addition, claims 1, 2, 5, 10, 12, and 14 were rejected under 35 U.S.C. 103(a) over Tseng in view of Sun and U.S. Patent No. 6,806,549 to Tomita; claim 3 was rejected under 35 U.S.C. 103(a) over Tseng in view of Sun, Tomita, and U.S. Patent Pub. No. 2002/0168830 to DeBoer et al.; claim 8 was rejected under 35 U.S.C. 103(a) over Tseng in view of Sun, Tomita, and U.S. Patent No. 6,010,955 to Hashimoto; claim 9 was rejected under 35 U.S.C. 103(a) over Tseng in view of Sun, Tomita, Hashimoto, and U.S. Patent No. 6,479,341 to Lu; claim 13 was rejected under 35 U.S.C. 103(a) over Tseng in view of Sun, Tomita, and U.S. Patent No. 5,817,562 to Chang et al.; claim 15 was rejected under 35 U.S.C. 103(a) over Tseng in view of Sun, Tomita, and U.S. Patent No. 5,779,927 to Lo; claims 16-19 were rejected under 35 U.S.C. 103(a) over Tseng in view of Sun, Tomita, and U.S. Patent Pub. No. 2002/0064968 to Kim et al.; and claim 20 was rejected under 35 U.S.C. 103(a) over Tseng in view of Sun, Tomita, and U.S. Patent No. 6,342,416 to Kim et al.

Claims 1-3, 5, 8-10, and 12-21 remain pending for consideration.

Claim 21

Claim 21 recites

> forming a gate on a device formation region of a semiconductor substrate, and forming source and drain regions in the device formation region of the semiconductor substrate *adjacent respective sides of the gate*, wherein the gate comprises a gate dielectric layer, a gate conductive layer and sidewall spacers located at respective sidewalls of the gate conductive layer; . . . [and]
>
> performing the dry etching process to etch the first interlayer insulating film *until portions of the etch stop layer disposed over the source region, the drain region and the sidewall spacers are exposed* to form self-aligned contact holes in the first interlayer insulating film over the source region and the drain region, respectively.

The Office Action admits that Tseng "fail[s] to teach performing the dry etching process to etch the first interlayer insulating film until portions of the etch stop layer disposed over the source region, the drain region and the sidewall spacers are

exposed." (See, Office Action at page 5, second paragraph). However, the Office Action then states

> Sun illustrates in FIG. 8, a method of plasma etching (same as dry etching) openings thru dielectric layer 94 to etch stop layer 90 and leaving portions of dielectric layer 96 over other parts of the device (column 8, line - column 9, line 3). One can see the other parts of the device include the sidewall 64, source/drain regions 80, 82, and 84, as shown in FIG. 8. Hence, the aforementioned reads on dry etching process to etch the first interlayer insulating film until portions of the etch stop layer disposed over the source region, the drain region and the sidewall spacers are exposed to form self-aligned contact holes in the first interlayer insulating film over the source region and the drain region.

(Office Action at page 5, fourth paragraph).

Sun discloses "gate electrodes 56," and discloses that "a layer 90 of etch stop material is disposed over the surface of the device." (See, Sun at column 7, lines 34-35 and at column 8, lines 12-13). Additionally, Sun discloses that "openings are etched through the interlayer dielectric 94," and that "this etch step preferably stops on the etch stop layer 90 and leaves portions of the dielectric layer 96 over other parts of the device." (See, Sun at column 8, lines 59-60 and at column 9, lines 1-3). However, it is apparent from FIG. 8 of Sun that after performing the etch step referred to above, dielectric layer 96 remains covering the portion of etch stop layer 90 disposed over source/drain region 82. Thus, Applicants submit that Sun, as relied upon, fails to disclose "performing the dry etching process to etch the first interlayer insulating film until portions of the etch stop layer disposed over *the source region, the drain region* and the sidewall spacers are exposed," as recited by claim 21. Claim 21 recites "forming source and drain regions in the device formation region of the semiconductor substrate *adjacent respective sides of the gate*". However, because FIG. 8 of Sun shows that dielectric layer 96 remains covering the portion of etch stop layer 90 disposed over source/drain region 82, Applicants submit that FIG. 8 of Sun *does not* show exposing portions of etch stop layer 90 disposed over a source region *and* a drain region disposed *adjacent respective sides of a gate*. For example, Applicants submit that FIG. 8 of Sun fails to show etching a first interlayer insulating film until portions of etch stop layer 90 disposed over a source region *and* a drain region *disposed adjacent respective sides* of a gate electrode 56 are exposed.

Claim 21 also recites "wet etching the buffer layer and the etch stop layer to expose *the source region, the drain region* and the first and second sidewall spacers." The Office Action admits that Tseng "fail[s] to teach . . . wet etching the buffer layer and the etch stop layer to expose the source region, the drain region and the sidewall spacers." (See, Office Action at page 5, third paragraph). However, the Office Action then states

> Sun also teaches plasma etching the etch stop layer 90 and alternatively wet etching the etch stop layer from within the openings in the dielectric layer. The latter etch step reads on wet etching the buffer layer and the etch stop layer. Sun further teaches after the etching steps not only the surfaces of the source, drain regions 80, 84 but also the spacer 64 are exposed (column 9, lines 5-8) which thereby reads on, wet etching the buffer layer and the etch stop layer to expose the source region, the drain region and the sidewall spacers.

(Office Action at page 5, fifth paragraph through page 6, first incomplete paragraph).

Sun discloses that "[a]fter the etching steps, not only the surfaces of source/drain regions 80, 84 but also surfaces of the oxide layer 62 and the spacer 64 are preferably exposed and clean, as shown in FIG. 8." (See, Sun at column 9, lines 10-13). However, FIG. 8 of Sun shows that source/drain region 82 remains covered by etch stop layer 90 after the etching steps of Sun referred to in the above quotation from Sun. Thus, Applicants submit that Sun, as relied upon, fails to disclose "wet etching the buffer layer and the etch stop layer to expose *the source region, the drain region* and the first and second sidewall spacers," as recited in claim 21, wherein the source and drain regions are formed adjacent respective sides of a gate, as recited by claim 21. For example, FIG. 8 of Sun fails to show etching etch stop layer 90 to expose a source region *and* a drain region *formed adjacent respective sides* of a gate electrode 56.

Therefore, Applicants submit that claim 21 should be allowed over the proposed combination of Tseng and Sun set forth in the Office Action for at least the reasons set forth above.

Claim 1

Claim 1 recites

> forming a gate on a device formation region of a semiconductor substrate, and *forming source and drain regions in the device formation*

region of the semiconductor substrate adjacent respective sides of the gate, wherein the gate comprises a gate dielectric layer, a gate conductive layer and sidewall spacers located at respective sidewalls of the gate conductive layer; . . . [and]

dry etching the first interlayer insulating film until portions of the etch stop layer disposed over *the source region, the drain region and the sidewall spacers are exposed* to form self-aligned contact holes in the first interlayer insulating film over the source region and the drain region, respectively.

Regarding claim 1, the Office Action states "[a]s to claims 1 and 5, Tseng discloses a method of fabricating a semiconductor memory device as described above in claim 21." (See, Office Action at page 6, fourth full paragraph). Although not stated explicitly, applicants assume that the Office Action intended to use the grounds set forth by the Office Action for rejecting claim 21 over Tseng and Sun in the rejection of claim 1. As discussed above with regard to claim 21, it is clear that the combination of Tseng, Sun, and Tomita set forth in the Office Action fails to fully teach or suggest the invention recited in claim 1. Accordingly claims 1-3, 5, 8-10, and 12-20 are allowable over the art of record.

Applicants respectfully request reconsideration and allowance of the pending claims.

Respectfully submitted,
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